Agile, eXtensible, fast I/O Module for the cyber-physical era

Road2CPS

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Brief introduction to the AXIOM project

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AXIOM OBJECTIVES

• OBJ1) Realizing a small board that is flexible, energy efficient and modularly scalable
  – Flexibility: FPGA provides acceleration, custom interconnects, ability to distribute threads across boards
  – Energy efficiency: low-power ARM, FPGA
  – Modularly scalable: fast+inexpensive interconnects based on SATA/USB-C, distributed shared memory across boards

• OBJ2) Easy programmability of multi-core, multi-board, FPGA
  – Programming model: Improved OmpSs
  – Runtime & OS: improved thread management

• OBJ3) Leveraging Open-Source software to manage the board
  – Compiler: BSC Mercurium
  – OS: Linux
  – Drivers: provided as open-source by partners

• OBJ4) Easy Interfacing with the Cyber-Physical World
  – Cyber-Physical World: integrating Arduino support for a plenty of pluggable board (so-called “shields”)
  – Platform: building on the UDOO experience from SECO

• OBJ5) Enabling real time movement of threads
  – Runtime: will leverage the EVIDENCE’s SCHED_DEADLINE scheduler (i.e. EDF) included Linux 3.14, UNISI’s low-level dataflow-based thread management techniques

• OBJ6) Contribution to Standards
  – Hardware: SECO is founding member of the Standardization Group for Embedded Systems (SGET)
  – Software: BSC is member of the OpenMP consortium
EASY PROGRAMMABILITY
VIA OPENMP-SS (OMPSS)

Only 3 lines of code to
- accelerate code on FPGAs
- distributed code across
  several AXIOM boards

```
1 #pragma omp target device(fpga, smp) copy-deps
2 #pragma omp task in(a[0:64*64-1], b[0:64*64-1]) out(c[0:64*64-1])
3 void matrix_multiply(float a[64][64],
4    float b[64][64],
5    float out[64][64]) {
6        for (int ia = 0; ia < 64; ++ia)
7            for (int ib = 0; ib < 64; ++ib) {
8                float sum = 0;
9                for (int id = 0; id < 64; ++id)
10                    sum += a[ia][id] * b[id][ib];
11                out[ia][ib] = sum;
12            }
13        }
14 }
15 ...
16 int main( void ){
17 ...
18 matrix_multiply(A,B,C1);
19 matrix_multiply(A,B,C2);
20 matrix_multiply(C1,B,D);
21 ...
22 #pragma omp taskwait
23 }
```

<table>
<thead>
<tr>
<th>Application</th>
<th>Seq - DMA version</th>
<th>pthread version</th>
<th>OmpSS version</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cholesky</td>
<td>71</td>
<td>26</td>
<td>3</td>
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<tr>
<td>Covariance</td>
<td>94</td>
<td>29</td>
<td>3</td>
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<tr>
<td>64x64</td>
<td>95</td>
<td>39</td>
<td>3</td>
</tr>
<tr>
<td>32x32</td>
<td>95</td>
<td>39</td>
<td>3</td>
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CAN WE DO THAT?

- SECO/UNISI achievements:
  - 2014: UDOO-ARM (99 $ PC+Arduino) → 600k$ on Kickstarter
  - 13th April 2016: UDOO-x86 (PC+Arduino, 10x faster than Raspberry-3) → 100k$ in 7 hours (!) on Kickstarter
FIRST PROTOTYPE UNDER REVIEW

- Stackup definition
  - 10 layers PCB
  - HS/LS/power planes arrangement
- Placement
  - Achieve mechanical and electrical constraints
- Routing (WIP)
  - Design for power/signal integrity
- 3D model available
AXIOM – THE MODULE-v2

• KEY ELEMENTS
  – K1: ZYNQ FPGA (INCLUDES 6 ARM CORES)
  – K2: ARM GP CORE(S)
  – K3: HIGH-SPEED & INEXPENSIVE INTERCONNECTS
  – K4: SW STACK – OMPSS+LINUX BASED
  – K5: OTHER I/F (ARDUINO, USB, ETH, WIFI, …)
CONSORTIUM EXPERTISE

• VIMAR, HERTA – 2 KILLER APPLICATIONS
• SECO – hardware module realization
• FORTH – high-speed interconnects
• EVI – Runtime, OS (Linux 3.14 real time scheduler)
• BSC – programming models
• UNISI – simulation, evaluation, coordination, architecture
WORKPACKAGES

• WP1: **Management** – UNISI (leader-Macy-project manager),
  ALL partners (mandatory)
• WP2: **Dissemination and Exploitation** – UNISI (leader-Caporali),
  ALL partners
• WP3: **Scenario Definition and App. Porting** – UNISI (leader-Rizzo),
  VIMAR, HERTA
• WP4: **Programming Model** – BSC (leader-Martorell),
  EVI, FORTH, SECO, HERTA
• WP5: **Runtime and OS** – EVI (leader-Gai),
  BSC, FORTH, SECO, UNISI
• WP6: **Platform** – SECO (leader-Catani),
  BSC, EVI, FORTH, UNISI, VIMAR
• WP7: **Simulation and Evaluation** – UNISI (leader-Giorgi),
  ALL partners
CONCLUSION - AXIOM IMPACT

• Realize a prototype module “ready-for-market”
  – VIMAR, HERTA first customers
  – for the public afterwards

• Strengthen European industry and research
  – in the supply, operate and use of Embedded Systems, achieving world-leadership
  – development of autonomous technology

• Development of extreme-performance system software and tools
  – European research at the forefront
TOWARDS
HPC + EMBEDDED CONVERGENCE
Agile, eXtensible, fast I/O Module for the cyber-physical era

PROJECT ID: 645496